Architetture degli Elaboratori II
II Test - 5/6/2003

First Name, Name :

Each exercise reports its value in marks: total marks 33/30.

1. (marks: 6)
   Describe which methods are usually implemented to reduce pipeline penalties in branch instructions. Describe the detailed implementation of a dynamic branch prediction table with 2 prediction bits on a CPU with 32 bit addresses, and indicate how many bits the table occupies.

2. (marks: 8)
   A possible IJVM instruction with indirect addressing mode could be the following:

   indload <varnum>

   where the memory cell addressed by <LV + varnum> contains the offset with respect to LV of the cell to push on the stack. Assuming that varnum is a 8 bit displacement, write for this new instruction:

   (a) the μ-interpreter MIC-1;
   (b) the μ-interpreter MIC-2.
   (c) the μ-interpreter MIC-3.

   Compare the execution times in the three cases.

3. (marks: 6)

   What is the addressing mode in a ISA instruction ?
   Assuming to have a CPU with 32 registers, numbered from R0 to R31, and considering an instruction MOV R1 <OP> that moves the operand <OP> in the register R1, indicate which are the most common addressing modes and how they affect the memory and the registers.

4. (marks: 8)
   Consider a CPU of last generation with 64 bit addresses. The main memory of the machine is organized as an array of 1 byte cells. byte.

   The space on the chip that can be allocated to the cache can contain 8K blocks of 128 bytes.

   Draw the structure of the cache and compute its total occupancy in bits for the following design alternatives:

   (a) direct mapped;
   (b) 2-ways set associative;
   (c) 4-ways set associative;
   (d) fully associative.

5. (marks: 5)
   Describe the main structure of the prefetching unit in the MIC-2 architecture, and illustrate in details:

   (a) why there are two MBR registers;

   (b) if it could be convenient to increase the dimension of the shift register;

   (c) draw the finite state machine representing the operation of the shift register with 8 positions.